CP2-DCDG-MRC

100G/200G CFP2 DCO Optical Transceiver

Features

- Maximum operating rate of 211.45Gbps
- Modulation format PM-QPSK (100G), PM-16QAM (200G)
- 100GE, OTU4 / OTUCn service access
- Hot-swappable CFP2 package
- Electrical interface supports OTL4.4, FOIC1.4, CAUI-4, and OTLC2.8
- Support the protocol "CFP2 MSA Hardware Specification 1.0 with modifications"
- Support the protocol "CFP MSA Management Interface Specification 2.2 with modifications"
- Optional proximal distal data loop back
- Support for OTN framer and Ethernet MAC / PCS
- Supports LLDP packet listening
- Maximum power consumption of 24W

Applications

- 100GbE IEEE 802.3bj;
- ITU-T G.709/Y.1331 for Optical transport network
- Switch to switch interface or Switch to router interface
- Access, Metro, Long-haul Ethernet DWDM Networks

Description

The Coherent 100G/200G CFP2-DCO optical module, using a 104pin CFP2-MSA connector,

serves as an electrical interface to the system board. The physical diagram of the module is shown in Figure :

module physical diagram

The module is mainly divided into three main functions: DSP, optical device and control unit. All the control interface pins are implemented by the internal control unit, which can also be used for the terminal modulator control, software management, and alarm performance reporting.

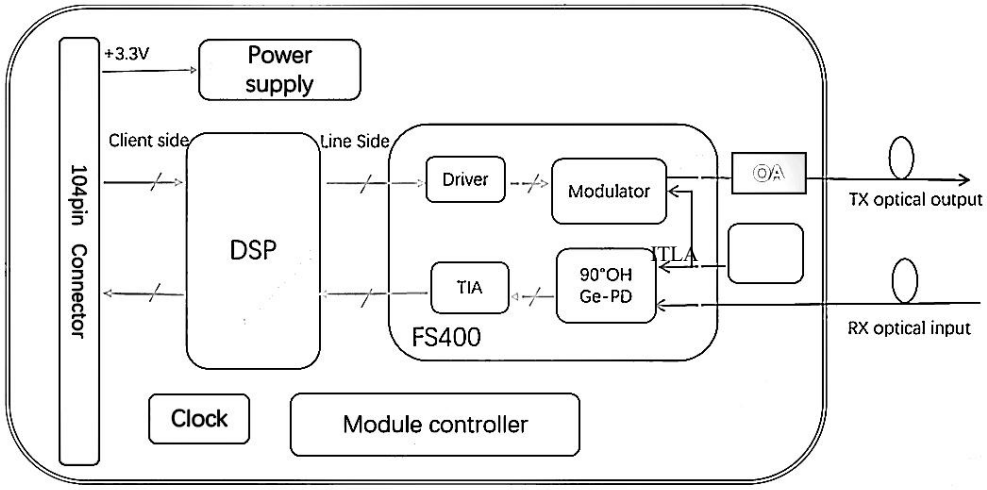

Figure Functional block diagram of the coherent CFP 2-DCO optical moduleperformance index

1.1 Optical port characteristics-100G

Table 1 Description of the 100 G optical port performance indicators

parameter	Performance value
Optical interface type	PM-QPSK

Number of wavelength channels	96 Wave
wavelength interval	50GHz
wavelength frequency range	191.3～196.05THz
wavelength stability	±1.5GHz
Output optical power default value	0dBm
Output power is a configurable power with a maximum value	+5dBm
The output power can be configured with a minimum value	-10dBm
Output power configuration accuracy	+/-1.5dB
Output Optical power during wavelength regulation	<-35dBm
CD tolerance	±40,000ps/nm
Maximum average DGD tolerance	50ps
Input the optical power range	0～-18dBm
OSNR tolerances (BOL)	11.5dB (received Optical power-8~ -10dBm)
power dissipation	Typ：22W；Max：24W

1.2 Optical port characteristics-200G

Table 2 Description of 200 G optical port performance indicators

parameter	Performance value
Optical interface type	PM-16QAM　PS
Number of wavelength channels	96 Wave
wavelength interval	50GHz
wavelength frequency range	191.3～196.05THz
wavelength stability	±1.5GHz
Output optical power default value	0dBm
Output power is a configurable power with a maximum value	+5dBm
The output power can be configured with a minimum value	-10dBm

Output power configuration accuracy	+/-1.5dBm
Output Optical power during wavelength regulation	<-35dBm
CD tolerance	±40,000ps/nm
Maximum average DGD tolerance	22ps
Input the optical power range	0～-18dBm
OSNR tolerances (BOL)	17.5dB (received Optical power-8~ -10dBm)
power dissipation	Typ：22W；Max：24W

2 Electrical characteristics

2.1 Power supply requirements

The coherent CFP2 optical module is powered by a separate 3.3V power supply coming from the motherboard. The internal device power supply of the optical module is converted from 3.3V power supply. The 3.3V power supply requirements are shown in Table 3. All the voltages are tested at the connector interface.

Table 3 Power supply characteristics of Coherent CFP2 optical module

parameter	Signal name	least value	representative value	crest value	unit	remarks
The 3.3V DC power supply voltage is provided	VCC	3.2	3.3	3.4	V	
The 3.3V DC power supply current	ICC			8.7	A	Remarks 1 & 2
power supply noise	Vrip			2	%p-p	DC – 1MHz
				3		1 – 10MHz
Power power consumption	Pw_class 4		26	29	W	400G pattern
working temperature	T	0		70	°C	

Note: The maximum minimum parameter value describes the full temperature range of the module life. Typical parameter values describe the operating temperature of 25°C, normal power supply, and life start indicators.

Note 1: The maximum current value of each pipe pin shall not exceed 1.3A.

Note 2: The maximum value of the Icc is for the design reference, and the normal operating current cannot exceed the Pw_normal / Vcc.

2.2 High-speed electrical interface index

The coherent CFP2 optical module can support a variety of electrical interfaces, as shown in Table 4

Table 4. Coherent CFP2 optical module

Client Type	Interface Type	Electrical Standards
100GE	CAUI-4	IEEE 802.3bm CAUI-4 Chip-to-Module
100GE	100GAUI-2	IEEE 802.3bm GAUI-8 Chip-to-Module
OTU4	OTL4.4	OIF CEI-28G VSR
OTUC1/OTUC2	FOIC1.4(FlexO-SR)	OIF CEI-28G VSR

2.2.1. Reference Clock (REFCLK)

The coherent CFP2 optical module does not require the motherboard to provide a reference clock REFCLK of 1 / 16.

2.2.2 Terminal Monitoring Clock (TXMCLK)

The coherent CFP2 optical module hair terminal can selectively provide a monitoring clock TXMCLK, mainly for monitoring the hair terminal Optical signal as a reference. The clock can be used to trigger a high-speed sampling oscilloscope.

Table 5 The Terminal Monitoring Clock (TXMCLK) Characteristics

parameter	Signal name	least value	representative value	crest value	unit	remarks
impedance	Zd	80	100	120	Ω	
The terminal monitoring clock frequency			1/48		Hz	The frequency is 1 / 48 of the symbol rate of the terminal

TXMCLK						Optical signal
TXMCLK differential voltage	V_{DIFFTX}	500		1000	mV	Differential peak peak voltage

2.3.Function description of control pin (non-MDIO port)

2.3.1.1 Non-enable pin (TX_DIS)

Terminal non-enabling pin TX_DIS is an input pin from the motherboard that works in a logical high-level state. When TX_DIS is a logical high level, the output Optical signal inside the optical module is turned off. When TX_DIS is a logic low level, the output Optical signal inside the Optical module is turned on. The timing of the TX_DIS is shown in Figure 7. On time t_on and off time t_off value are shown in Figure 3.

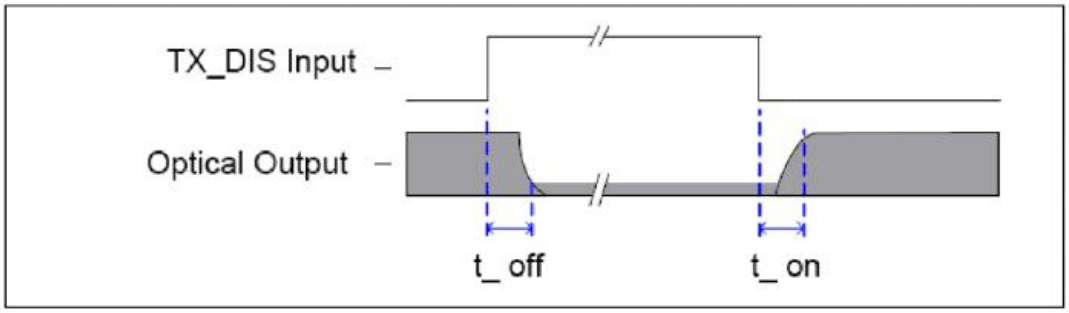

FIG. 3 Time diagram of transmission terminal nonenable signal TX_DIS

2.3.2 Module Low-power pin (MOD_LOPWR)

The optical module low-power pin (MOD_LOPWR) is an input pin from the mainboard that works in a logical high-level state. When the MOD_LOPWR is at a high level, the optical module is in a low-power mode and remains in this mode. When MOD_LOPWR is pulled down, the internal optical module is internally initialized into high power mode or normal operation mode. In the low-power mode, the optical module communicates through the MDIO management interface, and the maximum power consumption of the module does not exceed 2W. The MOD_LOPWR pin timing diagram is shown in Figure 8, with the t_MOD_LOPWR_on and _ t_ MOD_LOPWR_off values shown.

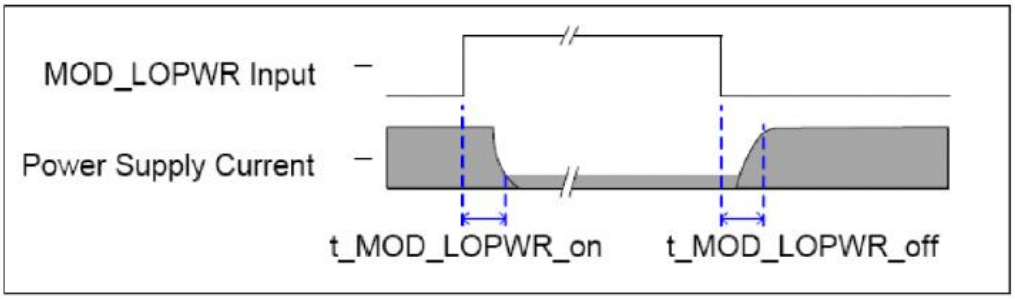

Figure 4 MOD_LOPWR timing diagram of module low power mode

2.3.3 Module reset pin (MOD_RSTn)

The optical module reset pin MOD_RSTn is an input pin from the motherboard and works in a logic-low-level state. When the MOD_RSTn is pulled to low levels, the optical module is reset. When the MOD_RSTn is a high level, the optical module exits the reset mode and starts the module overpower initialization process.

2.4 Function description of alarm pin (non-MDIO port)

2.4.1 Lost receiver signal alarm pin (RX_LOS)

The receiver signal loss alarm pin RX_LOS is an output output pin connected to the mainboard and operates in a logical high-level state. When RX_LOS is a logical high level, it indicates that the optical module receives the optical power that is too low. The timing of the RX_LOS pins is shown in Figure 5.

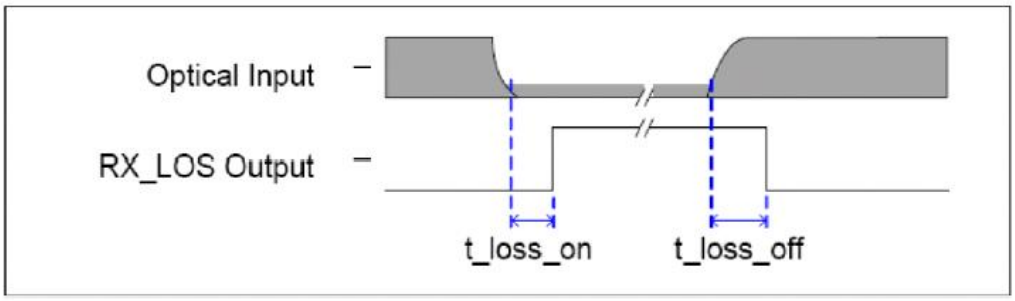

FIG. 5 Lost signal alarm RX_LOS timing diagram

2.4.2 Optical module is not in place alarm pin (MOD_ABS)

Optical module without in-place alarm pin MOD_ABS is an output pin connected to the motherboard from the internal output of the module, which is pulled up on the motherboard and pulled down to the ground inside the module. When the optical module is inserted into the

motherboard, MOD_ABS is a logical low level indicating that the module is in place; when the optical module is absent on the motherboard, MOD_ABS is a logical high level indicating that the module is not in place.

2.4.3 Description of control and alarm

2.4.3.1 Control and alarm signal timing parameters

Table 6. Summary of the signal timing parameters

parameter	signal	least value	representative value	crest value	unit
Terminal not enabled (TX_DIS is high level)	t_off			100	us
Terminal enable (TX_DIS is low level)	t_on			25	s
MOD_LOPWR assert	t_MOD_LOPWR_assert			9.5	s
MOD_LOPWR deassert	t_MOD_LOPWR_deassert	0.1		10	s
Receiver Loss of Signal Assert Time	t_loss_on	0.5		400	us
Receiver Loss of SignalDe-assert Time	t_loss_off	0.5		400	us
Initialization time from Reset	t_initialize	19		150	s

2.4.3.2Control and alarm pins: 3.3V LVCMOS electrical characteristics

The 3.3V LVCMOS level of the above hardware control and alarm signal pins must meet the electrical characteristics as shown in Table 7. Figure 6 shows the recommended input-output end reference methods for these pins.

Table 7 3.3 Electrical Characteristics of V LVCMOS

parameter	signal	least value	representative value	crest value	unit
service voltage	VCC	3.2	3.3	3.4	V
Enter high voltage	VIH	2		VCC+0.3	V
Input low voltage	VIL	-0.3		0.8	V
Input the leakage current	IIN	-10		10	uA
Output high voltage (I_{OH}=-100uA）	VOH	VCC-0.2			V
Output low voltage (I_{OL}=100uA）	VOL			0.2	V

Figure 2-6: Reference +3.3V LVCMOS Output Termination

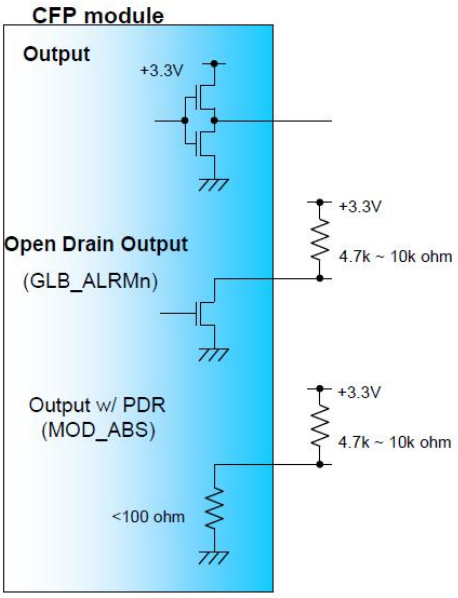

Figure 2-7: Reference +3.3V LVCMOS Input Termination

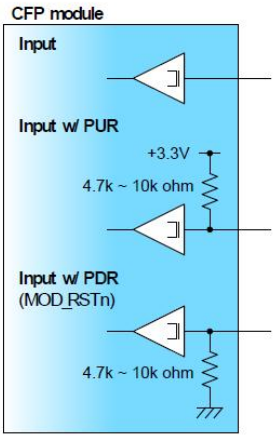

Figure 6 3.3V LVCMOS Input / Output Reference End Mode

2.5 Module Management Interface (MDIO) Description

2.5.1 Management data input / output interface (MDIO)

MDIO is defined by clause 45 of IEEE802.3. The MDIO of the optical module uses a 1.2V LVCMOS logic level.

2.5.2 Management data clock pin (MDC)

For the MDIO and MDC pin timing chart, see Figure 7. The optical module shall follow the minimum establishment time tsetup and hold time thold value requirements of the MDIO port supplement protocol.

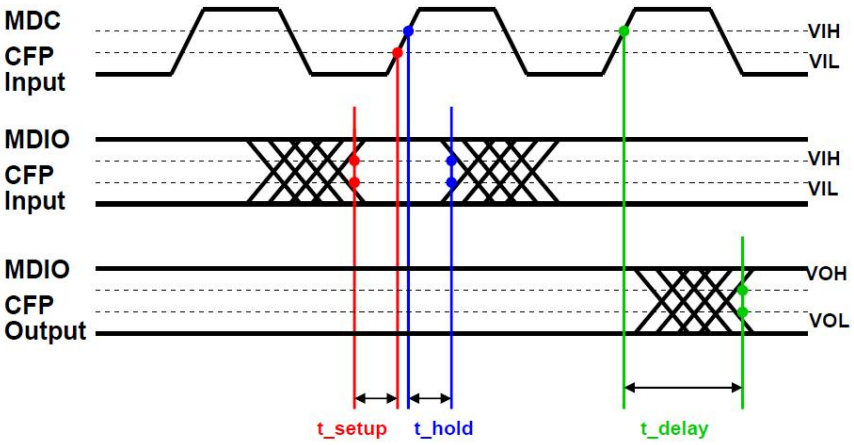

Figure 7 Time diagram of optical module MDIO & MDC interface

Note: Test it on the MDIO & MDC pins of the optical module.

2.5.3 MDIO Physical Interface Address Foot (PRTADRs)

The MDIO physical interface address pin PRTADRs is used by the motherboard system to assign addresses to all of the optical modules contained in its management area. PREADR0 corresponds to the LSB of the physical interface address bit. The main board drives the physical interface address line of 5pin to set the physical interface address of the optical module. The physical interface address of the optical module should follow the address protocol of the MDIO port. It is recommended that these physical interface address should not change when the optical module is powered on.

2.5.4 MDIO interface pin: 1.2V LVCMOS electrical characteristics

The MDIO pins described above in 1.2V LVCMOS mode shall meet the electrical characteristics described in Figure 17. Table 8 describes the input-output termination mode of the recommended reference pins.

Table 8 1.2 Electrical Characteristics of V LVCMOS

parameter	signal	least value	representative value	crest value	unit
Enter high voltage	VIH	0.84		1.5	V
Input low voltage	VIL	-0.3		0.36	V
Input the leakage current	IIN	-100		100	uA
Output high voltage (I_{OH}=-100uA）	VOH	1		1.5	V
Output low voltage (I_{OL}=100uA）	VOL	-0.3		0.2	V
Output high current	IOH			-4	mA
Output low current	IOL	+ 4			mA
input capacitance	Ci			10	pF

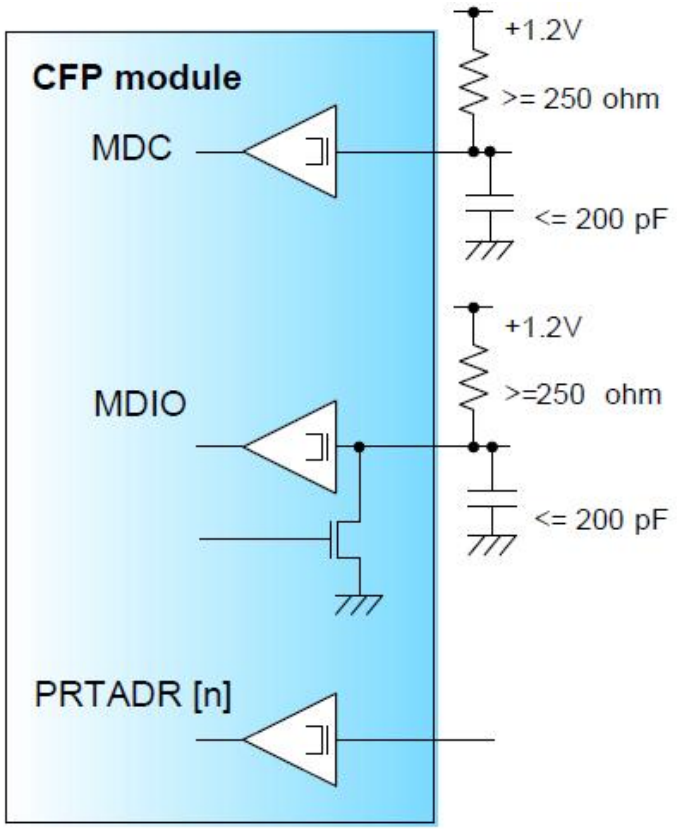

Figure 8. M D I O interface reference termination mode

3. Common registers

Table 9 Register List

Hex Addr	Size	Access Type	Bit	Register Name Bit Field Name	Description
B016	1	RO		Module State	CFP module state.Only a single bit set at any time.
			15~9	Reserved	
			8	High-Power-down State	1: Corresponding state is active.Word value = 0100h.
			7	TX-Turn-off State	1: Corresponding state is active.Word value = 0080h.
			6	Fault State	1: Corresponding state is active.Word value = 0040h. (Also referred to as MOD_FAULT)
			5	Ready State	1: Corresponding state is active.Word value = 0020h.

					(Also referred to as MOD_READY)
			4	TX-Turn-on State	1: Corresponding state is active.Word value = 0010h.
			3	TX-Off State	1: Corresponding state is active.Word value = 0008h.
			2	High-Power-up State	1: Corresponding state is active.Word value = 0004h.
			1	Low-Power State	1: Corresponding state is active.Word value = 0002h.
			0	Initialize State	1: Corresponding state is active.Word value = 0001h.
818A	2	RO	15~0	TX/RX Minimum Laser Frequency 1	An unsigned 16-bit integer with LSB = 1THz.MSB stored at low address.LSB stored at high address.
818C	2	RO	15~0	TX/RX Minimum Laser Frequency 2	An unsigned 16-bit integer with LSB = 0.05 GHz.Value should not exceed 19999. MSB stored at low address.LSB stored at high address.
818E	2	RO	15~0	TX/RX Maximum Laser Frequency 1	An unsigned 16-bit integer with LSB = 1THz.MSB stored at low address.LSBstored at high address.
8190	2	RO	15~0	TX/RX Maximum Laser Frequency 2	An unsigned 16-bit integer with LSB = 0.05 GHz.Value should not exceed 19999. MSB stored at low address.LSB stored at high address.
B400	1 (16)			TX Channel Control	Desired TX channel number and grid spacing.16 registers, one for each network lane,represent 16 network lanes.n = 0, 1,…,N-1. N_max = 16. Actual N is module dependent.
		RW	15~13	Grid Spacing	000b: 100 GHz grid spacing 001b: 50 GHz grid spacing 010b: 33 GHz grid spacing 011b: 25 GHz grid spacing 100b: 12.5 GHz grid spacing 101b: 6.25 GHz grid spacing 110b ~ 111b: Reserved
		RO	12~11	Reserved	
		RW	10	Enabled Arbitrary Settable Tx Minimum Laser Frequency Registers	0: Disabled. 1: Enabled, With this bit set to Enabled the high resolution registers detailed in Section 12.6 of Addendum A shall be used

		RW	9~0	Channel number	Tx channel number.Channel 0 is an undefined channel number.
B450	1(16)	RW	15~0	TX Frequency 1	Current module TX Frequency 1. An unsigned 16-bit integer with LSB = 1THz.
B460	1(16)	RW	15~0	TX Frequency 2	Current module TX Frequency 2. An unsigned 16-bit integer with LSB = 0.05GHz.Value should not exceed 9999.
B470	1(16)	RW	15~0	RX Frequency 1	Current module RX Frequency 1. An unsigned 16-bit integer with LSB = 1THz.
B480	1(16)	RW	15~0	RX Frequency 2	Current module RX Frequency 2. An unsigned 16-bit integer with LSB = 0.05GHz.Value should not exceed 9999.
B010	1			Module General Control	
		RW/SC/ LH	15	Soft Module Reset	Register bit for module reset function.Writing a 0 to this bit has no effect regardless if it was 0 or 1 previously. 1: Module reset asserted.
		RW	14	Soft Module Low Power	Register bit for module low power function. 1: Asserted.
		RW	13	Soft TX Disable	Register bit for TX Disable function. 1: Asserted.
		RW	12	Soft PRG_CNTL3 Control	Register bit for PRG_CNTL3 control function. 1: Asserted.
		RW	11	Soft PRG_CNTL2 Control	Register bit for PRG_CNTL2 control function. 1: Asserted.
		RW	10	Soft PRG_CNTL1 Control	Register bit for PRG_CNTL1 control function. 1: Asserted.
		RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal.When this bit is asserted it generates GLB_ALRM signal.1: Asserted.
		RW/SC	8	Processor Reset	Register bit for processor reset function.This bit is self-clearing.Register settings are not affected.This is a Non-Service Affecting reset.1: Asserted.
		RO	7~6	Reserved	
		RO	5	TX_DIS Pin State	Logical state of TX_DIS pin.1: Asserted

		RO	4	MOD_LOPWR Pin State	Logical state of MOD_LOPWR pin.1: Asserted
		RO	3	PRG_CNTL3 Pin State	Logical state of PRG_CNTL3 pin.1: Asserted
		RO	2	PRG_CNTL2 Pin State	Logical state of PRG_CNTL2 pin.1: Asserted
		RO	1	PRG_CNTL1 Pin State	Logical state of PRG_CNTL1 pin.1: Asserted
		RO	0	Reserved	

4. work environment

Table 10 Description of the working environment

parameter	minimum	maximum	unit	remarks
Storage temperature	-40	85	°C	
Operating Temperature-Case	0	70	°C	
relative humidity	5	85	%	
Relative humidity- -Absolute Maximum	5	95	%	
ESD HBM		High-speed pipe pin: 500V Other pipe pins: 2K	V	

5. Foot distribution and description

For 104pin electrical connection, in addition to 8 TX differential signal (TXI of this signal is the input of the module, the signal output of the disk), 8 RX differential signal (this signal is the output of the module and the signal input of the disk), starting direction 1 monitoring clock, control pin, alarm pin, MDIO communication related pin, and GND, +3.3V power supply.+ 3.3V Power supply maximum 1.3A per pin.

Table 11 Pipe foot definition-non-high speed pins

Pin	Bottom	I/O	Logic	Comment
1	GND	GND	Ground	Module Ground. Logic and power return path
2	OHIO_RDn	O	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base-X SerDes, AC coupling inside modules
3	OHIO_RDp	O	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base-X SerDes, AC coupling inside modules
4	GND	GND		Module Ground. Logic and power return path
5	OHIO_TD0n	I	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base-X SerDes, AC coupling inside modules
6	OHIO_TD0p	I	CML	The Overhead Access Interface, 1.25Gbps SGMII/2500Base-X SerDes, AC coupling inside modules
7	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
8	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
9	3.3V	PWR		
10	3.3V	PWR		
11	3.3V	PWR		
12	3.3V	PWR		
13	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
14	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
15	VND_IO_A	I/O		Customers must not connect to any of the VND_IO_x pins unless specifically allowed to do so
16	VND_IO_B	I/O		Customers must not connect to any of the VND_IO_x pins unless specifically allowed to do so
17	PRG_CNTL1	I	LVCMOS w/PUR	Internal 10k pull-up; TRXIC_RSTn
18	PRG_CNTL2	I	LVCMOS w/PUR	Internal 10k pull-up; Hardware Interlock LSB
19	PRG_CNTL3	I	LVCMOS w/PUR	Internal 10k pull-up; Hardware Interlock MSB
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1; MSA Default "H" = HIPWR_ON
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2; MSA Default "H" = MOD_READY
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 2; MSA Default "H" = MOD_READY
23	GND	GND	Ground	Module Ground. Logic and power return path
24	TX_DIS	I	LVCMOS w/PUR	Transmitter disabled for all lanes. Internal 10k pull-up;
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal; Internal 4.7k pull-up.
26	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power; Internal 10k pull-up;
27	MOD_ABS	O	GND	Module Absent; Internal 50Ω pull-down;
28	MOD_RSTn	I	LVCMOS w/PDR	Module Reset; Internal 10k pull-down;
29	GLB_ALRMn	O	LVCMOS	Global Alarm "H" = Alarm; "L" = OK
30	GND	GND	Ground	Module Ground. Logic and power return path
31	MDC	I	1.2V CMOS	MDIO Clock input
32	MDIO	I/O	1.2V CMOS	Management Data Input Output.
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port Address bit 0
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port Address bit 1
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port Address bit 2
36	VND_IO_C	I/O		Customers must not connect to any of the VND_IO_x pins unless specifically allowed to do so
37	VND_IO_D	I/O		Customers must not connect to any of the VND_IO_x pins unless specifically allowed to do so
38	VND_IO_E	I/O		Customers must not connect to any of the VND_IO_x pins unless specifically allowed to do so
39	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
40	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
41	3.3V	PWR		
42	3.3V	PWR		
43	3.3V	PWR		
44	3.3V	PWR		
45	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
46	3.3V_GND	GND	Ground	Power Ground. Internally connected to GND. Logic and power return path.
47	NC	NC	NC	
48	NC	NC	NC	
49	GND	GND	Ground	Module Ground. Logic and power return path
50	TXMONCLKN	O	CML	For optical waveform testing. Not for normal use
51	TXMONCLKP	O	CML	For optical waveform testing. Not for normal use
52	GND	GND	Ground	Module Ground. Logic and power return path

Table 12 Pipe Foot Definition-High-speed pipe pin

Pin	Top	I/O	Logic	Comment
104	GND	GND	Ground	Module Ground. Logic and power return path
103	TX4n	I	CML	
102	TX4p	I	CML	
101	GND	GND	Ground	Module Ground. Logic and power return path
100	TX3n	I	CML	
99	TX3p	I	CML	
98	GND	GND	Ground	Module Ground. Logic and power return path
97	TX2n	I	CML	
96	TX2p	I	CML	
95	GND	GND	Ground	Module Ground. Logic and power return path
94	TX5n	I	CML	
93	TX5p	I	CML	
92	GND	GND	Ground	Module Ground. Logic and power return path
91	TX6n	I	CML	
90	TX6p	I	CML	
89	GND	GND	Ground	Module Ground. Logic and power return path
88	TX1n	I	CML	
87	TX1p	I	CML	
86	GND	GND	Ground	Module Ground. Logic and power return path
85	TX0n	I	CML	
84	TX0p	I	CML	
83	GND	GND	Ground	Module Ground. Logic and power return path
82	TX7n	I	CML	
81	TX7p	I	CML	
80	GND	GND	Ground	Module Ground. Logic and power return path
79	(REFCLKn)	I	CML	
78	(REFCLKp)	I	CML	
77	GND	GND	Ground	Module Ground. Logic and power return path
76	RX4n	O	CML	
75	RX4p	O	CML	
74	GND	GND	Ground	Module Ground. Logic and power return path
73	RX3n	O	CML	
72	RX3p	O	CML	
71	GND	GND	Ground	Module Ground. Logic and power return path
70	RX2n	O	CML	
69	RX2p	O	CML	
68	GND	GND	Ground	Module Ground. Logic and power return path
67	RX5n	O	CML	
66	RX5p	O	CML	
65	GND	GND	Ground	Module Ground. Logic and power return path
64	RX6n	O	CML	
63	RX6p	O	CML	
62	GND	GND	Ground	Module Ground. Logic and power return path
61	RX1n	O	CML	
60	RX1p	O	CML	
59	GND	GND	Ground	Module Ground. Logic and power return path
58	RX0n	O	CML	
57	RX0p	O	CML	
56	GND	GND	Ground	Module Ground. Logic and power return path
55	RX7n	O	CML	
54	RX7p	O	CML	
53	GND	GND	Ground	Module Ground. Logic and power return path

6. machine design

The mechanical size definition of the coherent CFP 2-DCO optical module is shown in Figure 9.

The maximum module size is defined as: 107.5mm(L)*41mm(W)*12.4mm (H)..5

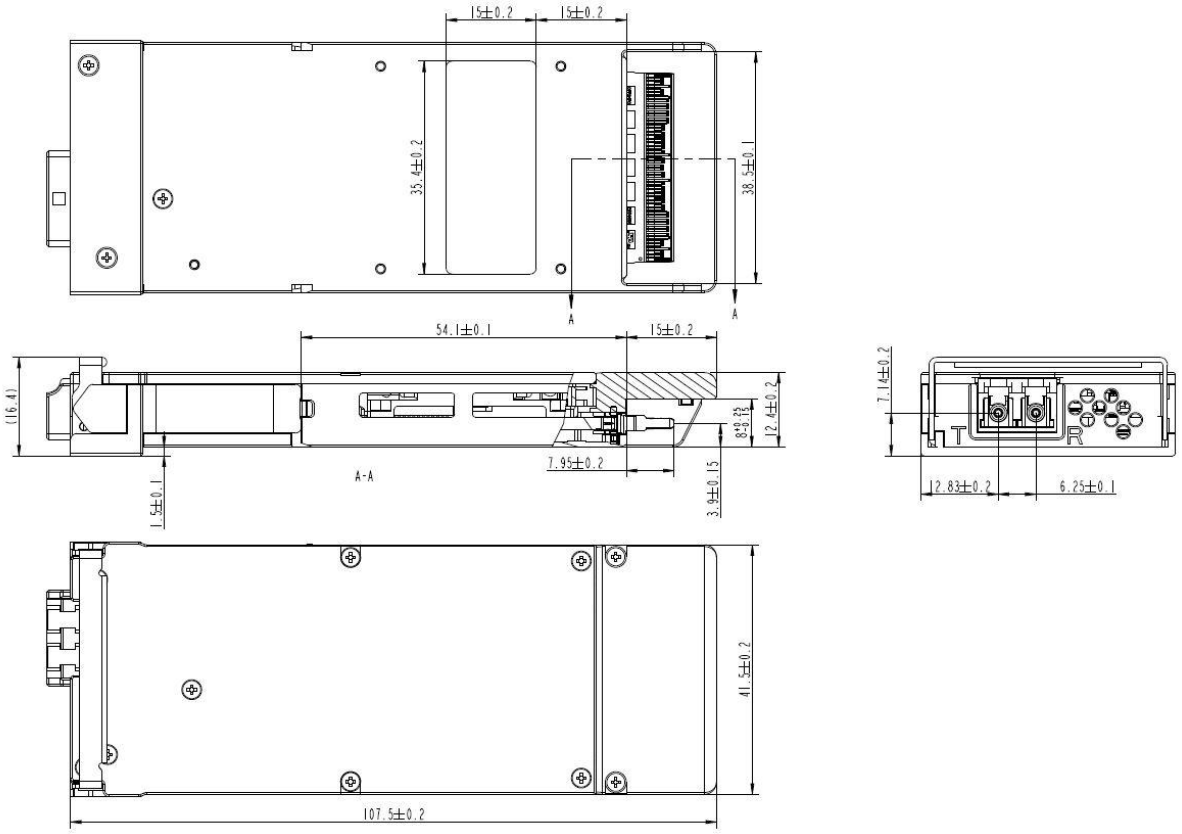

Figure 9 Mechanical dimensions of the C F P 2 optical module

7.Ordering information

Part Number	Product Description
CP2-DCDG-MRC	100G/200G, Optical CFP2-DCO

8.For More Information

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